

ABSTRACT

A computer chipset having an identifier module and a router. The identifier module is configured to add sequence identifiers to each transaction in independent ordered sequences of transactions. The sequence identifiers identify which ordered sequence the transactions belong to. The identifier module combines the ordered sequences of transactions into a combined ordered sequence of transactions. The combined ordered sequence of transactions are sent over an ordered interface. A router then separates the combined ordered sequence of transactions into ordered queues based on the sequence identifiers associated with the transactions. The transactions in the ordered queues are executed in an order that reduces the time required to complete the transactions.

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